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In this issue

Technology Developed in GICE

CMOS Devices and Circuits for THz Applications

from Electromagnetics Group

INTRODUCTION

THz science and technologies have attracted great attention in recent years because they can be used for many useful and unique applications, including high-speed wireless data communication, biomedical imaging, medicine analysis, chemical detection, and security screening. Using CMOS technologies to realize THz systems is especially appealing due to the benefits of low cost, high integration, and mass-production capability. We have developed several key CMOS devices and circuits which are good candidates to realize THz electronic systems.

CMOS THZ DEVICES AND CIRCUITS

A. High-Gain THz Dielectric Resonator Antenna (DRA)

The proposed THz DRA is shown in Fig. 1 [1], [2]. It is comprised of a dielectric resonator (DR) made of high-Z silicon material and an on-chip feeding patch realized in a 0.18-μm CMOS technology. The idea is to let the low-loss DR work as the radiating element while the on-chip patch operates as a feeding network. The proposed DRA can be employed to enhance the antenna gain of either a single element or a 2 2 antenna array. The measured antenna gain improvement of the proposed DRA over a conventional on-chip patch antenna can be 6.7 dB at 327 GHz. For antenna array improvement, the antenna gain enhancement can reach a value of 7 dB at 330 GHz.

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GICE Honors

Prof. Ai-Chun Pang
2021 IEEE Fellow

Prof. Tzong-Lin Wu
64th Academic Award of Ministry of Education

Message from the Director

Hsuan-Jung Su

Professor & GICE Director

All of a sudden, the COVID-19 outbreak escalates in Taiwan. Please do stay safe and healthy. In this issue, we would like to celebrate Prof. Ai-Chun Pang's election to 2021 IEEE Fellow and Prof. Tzong-Lin Wu receiving the 64th Academic Award of Ministry of Education. We feel honored and excited to have these outstanding professors with NTU GICE.

Our research sharing in this issue includes Prof. Chun-Hsing Li's research on CMOS Devices and Circuits for THz Applications, and Prof. Jiun-Lang Huang's research on Application of Machine Learning in Generating Self-Test Programs for Online Processor Testing. We are also excited to report the success of the first hybrid (in-person event joined by on-line attendees) flagship conference of the IEEE Communications Society (ComSoc), IEEE GLOBECOM 2020, hosted by GICE professors. On the student activities, we are happy to see the IEEE NTU Student Branch resuming operation led by GICE students. Please grab a coffee, relax and enjoy this issue.

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B. *Low-Loss Balun-Embedded THz Interconnect*

Fig. 2 shows the proposed balun-embedded THz interconnect which is a key component for a high-performance and low-cost THz heterogeneous system [3]. Two transmission lines are deployed on a 40-nm CMOS chip and an integrated-passive-devices (IPD) carrier, respectively. The chip is then flipped and bonded to the carrier using an Au-Au thermal-compressive technique with 5-μm thick gold bumps. By doing this, these two transmission lines can be coupled together to form coupled transmission lines. Moreover, the coupled lines are intentionally arranged to a Marchand balun structure. Therefore, the proposed interconnect not only can provide signal transition from the chip to the carrier, but it can also give single-ended to differential signal conversion. Two interconnects using the proposed idea are demonstrated with measured and simulated insertion loss of 0.9 and 1.4 dB at 169 and 340 GHz, respectively.

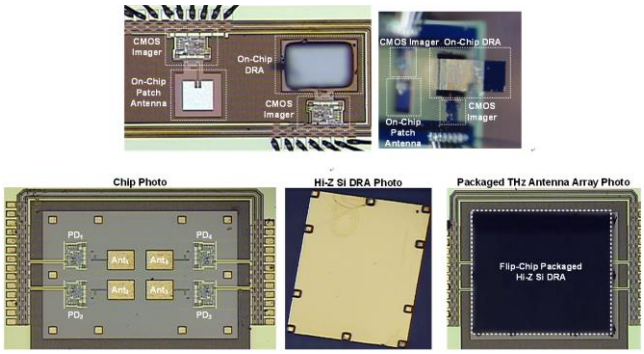

Fig. 1. Proposed THz dielectric resonator antennas.

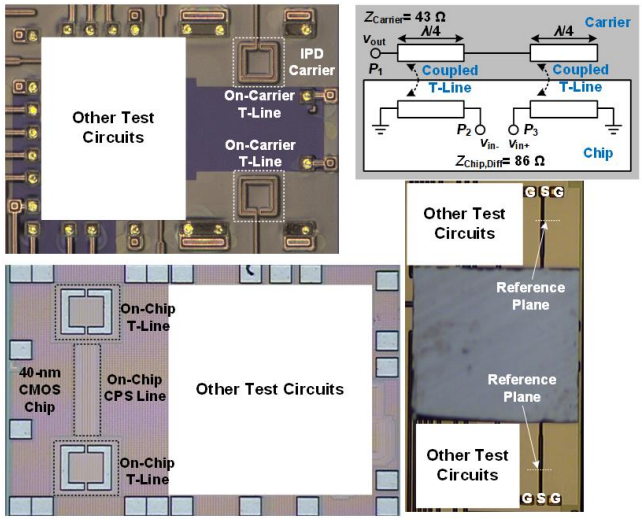

Fig. 2. Proposed balun-embedded THz interconnect.

C. *High-Performance Receivers and Frequency Doubler*

Fig. 3 depicts the proposed V-band frequency doubler (FD), W-band packaged receiver, and THz heterodyne receiver, which are key components for THz applications. The proposed FD can provide differential output without any additional balun required by manipulating the desired second harmonic current flows by a multifunction network [4]. Realized in a 90-nm CMOS technology, the proposed FD can give measured amplitude and phase imbalances of only 0.2 dB and 0.5°, respectively, while providing -5.5 dB conversion gain at the output frequency of 60 GHz. The proposed W-band receiver is composed of a 90-nm CMOS chip and an IPD carrier [5]. The chip which integrates a low-noise amplifier (LNA), a single-sideband mixer, a FD, and a wide-band variable-gain amplifier (VGA), is flip-chip packaged to the IPD carrier through a low-loss interconnect. Experimental results show that the proposed packaged receiver can provide 48.2-dB gain and 7.8-dB NF at 90 GHz while only dissipating 73.9 mW from a 1.2-V supply. The proposed THz heterodyne receiver consists

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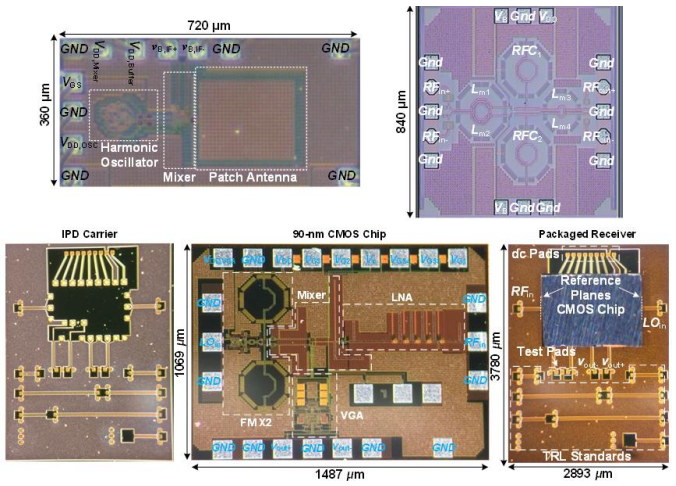

Fig. 3. Proposed THz receiver, V-band frequency doubler, and W-band packaged receiver.

of an on-chip patch antenna, a single-balanced mixer, and a triple-push harmonic oscillator [6]. The oscillator adopts a proposed harmonic oscillator architecture which can provide differential output by extracting output signals from the same current loop without any additional balun required. The mixer biased in the subthreshold region is designed not only to have high conversion gain and low noise figure, but the required LO power can also be as low as -11 dBm. Such a low demand on the LO power makes the proposed mixer very suitable for THz applications in which the achievable LO power is very limited. Realized in a 40-nm digital CMOS technology, the proposed THz receiver can provide measured voltage conversion gain of -1.7 dB at 335.8 GHz while only consuming 53.1 mW from a 1.1 V supply.

D. High-Resolution THz Transmissive Imaging System

The proposed THz receiver is employed to set up a transmissive THz imaging system as shown in Fig. 4 [6]. To test the spatial resolution of the established THz imaging system, the first DUT is selected as a tweezer. From the taken image, the resolution can be estimated to be 1.4 mm, close to the theoretical value of 1.1 mm according to the Rayleigh criterion. Another DUT chosen is a thin layer of pork with thickness of around 1 mm. The taken image illustrates that the THz signal can penetrate through the fat, but not the lean meat and muscle. This is due to the fact that muscle and the meat contain more water than the fat does.

CONCLUSION

Several key CMOS circuits and components, including high-gain DRAs, a power detector, a heterodyne receiver, and a balun-less

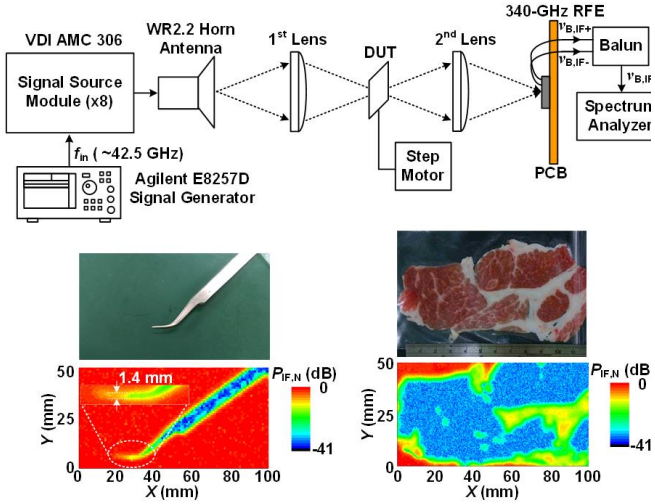

Fig. 4. Proposed THz transmissive imaging system.

frequency doubler, are presented. They not only show state-of-the-art performance, but also are set up with commercial transmitter modules, optical lens, and step motors, to successfully demonstrate THz transmissive imaging systems, implying high-performance and low-cost CMOS THz systems are going to be available in the near future.

REFERENCES

[1] C.-H. Li and T.-Y. Chiu, "340-GHz low-cost and high-gain on-chip higher-order dielectric resonator antenna for THz applications," IEEE Trans. THz Sci. Technol., vol. 7, no. 3, pp. 284-294, May 2017.

[2] C.-H. Li and T.-Y. Chiu, "Single flip-chip-packaged dielectric resonator antenna for CMOS terahertz antenna array gain enhancement," IEEE Access, vol. 7, pp. 7737-7746, 2019.

[3] T.-Y. Chiu, Y.-L. Lee, C.-L. Ko, S.-H. Tseng, and C.-H. Li, "A low-loss balun-embedded interconnect for THz heterogeneous system integration," IEEE Int. Microwave Symp., 2020.

[4] C.-H. Li et al., "A 340-GHz heterodyne receiver front-end in 40-nm CMOS for THz biomedical imaging applications," IEEE Trans. THz Sci. Technol., vol. 6, no. 4, pp. 625-636, Jul. 2016.

[5] C.-H. Li and W.-M. Wu, "A balun-less frequency multiplier with differential output by current flow manipulation," IEEE Trans. Very Large Scale Integr. Syst., vol. 26, no. 7, pp. 1391-1402, Jul. 2018.

[6] C.-H. Li, W.-T. Hsieh, and T.-Y. Chiu, "A flip-chip-assembled W-band receiver in 90-nm and IPD technologies," IEEE Trans. Microw. Theory Tech., vol. 67, no. 4, pp. 1628-1639, Apr. 2019.

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Technology

Application of Machine Learning in Generating Self-Test Programs for Online Processor Testing

from Data Science and Smart Networking Group

INTRODUCTION

Combining Artificial Intelligence (AI) and Internet of Things (IoT), AIoT devices have been bringing once infeasible services into being, and gradually reshaping our lives. One of the driving forces of AIoT is IC (Integrated Circuit) — with the advance of IC fabrication technology, designers are able to integrate ever growing functionalities into one single die or package that occupies smaller footprint and consumes less power than before. However, the penetration of AIoT into mission-critical applications also poses new challenges to IC testing — these applications demand not only zero DPPM (defective parts per million) at time zero but also high in-field reliability during their long lifetime expectancy.

Software-Based Self-Test for Processor Cores

For processor cores, Software-based self-test (SBST) is a promising solution to high in-field reliability. The idea is to have the processor under test (PUT) execute tailored self-test programs that aim to detect latent defects that escape manufacturing test or aging induced timing violations. The execution results are compared with stored fault-free responses to make the pass/fail decision. Compared to scan-chain based power-on self-test (POST) that requires switching PUT to the test mode, SBST is more flexible because it is a functional mode operation. In fact, SBST can even be viewed as one of the system routines.

Fig. 1 illustrates the processor self-test program generation flow that we developed. First, processor ISA (Instruction Set Architecture) is analyzed to obtain illegal processor states. They become constraints on the following ATPG (Automatic Test Pattern Generation) process to maximize the probability that the generated test patterns can be realized by instruction sequences. At the heart of the flow is the pattern-to-program conversion of which the goal is to synthesize instruction sequences that implicitly execute ATPG test patterns that were meant to be applied through scan operations. Test program templates are crucial to the conversion process. Each of them represents a processor behavior, e.g., forwarding, prediction, and out-of-order execution, and is utilized to bring the processor to the state as specified in a test pattern.

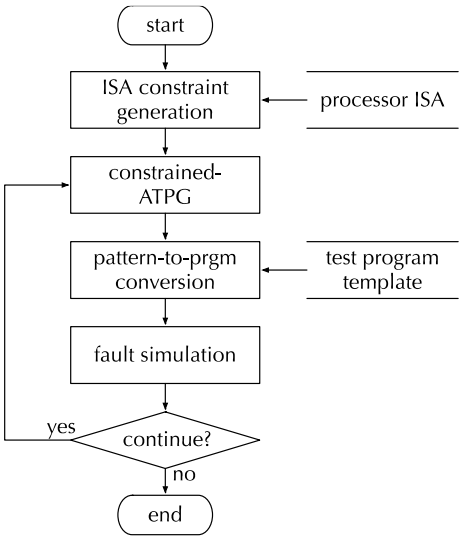

Fig. 1 The self-test program generation flow.

Machine Learning Assisted Test Program Template Generation

One major challenge to SBST is that it requires comprehensive PUT knowledge, ranging from ISA, architecture, to the RTL (register-transfer level) and gate-level designs. As a result, it involves intensive human efforts and is almost always realized in an ad hoc manner.

For the self-test program generation flow in Fig. 1, we currently focus on automating the generation of test program templates. Fig. 2 depicts the template generation flow where the shaded blocks are ML assisted. First, the "bounded random program generation" step produces program segments that are intended to discover unvisited or reach fault-detection states. Reinforcement learning (RL) is applied to evaluate past segments and adjust the random program generation strategy. For a MIPS32 processor core, preliminary results of RL-based test program generation is capable of activating more than 90% of target faults.

The execution traces from RTL simulation are divided into slices. For each of them, a corresponding data flow graph is constructed. There are two types of nodes in the graph: a value node represents a set of flip-flops and an operator node the involved data operation. Edges, on the other hand, indicates the data

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flow. To facilitate "graph clustering," the data flow graphs are simplified by merging interchangeable value nodes and generalizing operation nodes. Clustering techniques are applied to the resulting graphs to identify processor behavior. Not shown in Fig. 2, "data flow graph construction" and "graph clustering" iteratively update the node merging and generalization strategy to enhance behavior identification.

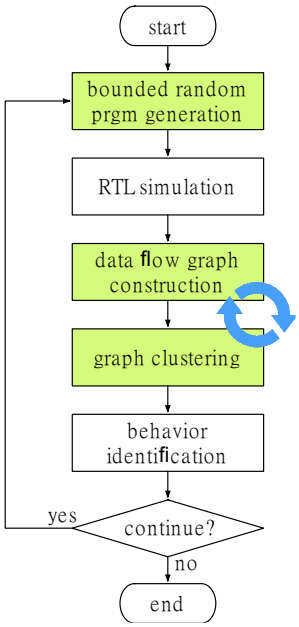

Fig. 2 The test program template generation flow.

A prototype self-test program generator has been implemented to validate the idea on a MIPS32 processor with 5-stage pipeline. Fig. 3 shows the achieved transition delay fault (TDF) coverage (PATIG, in red). The fault coverage is already 73.78% in the first iteration, and continues growing to be 97.82% after 36 iterations.

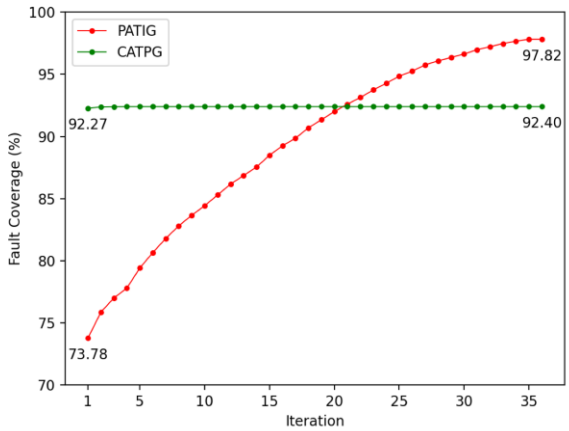

Fig. 3 TDF coverage (PATIG).

Conclusion

Processor reliability is crucial to the success of AIoT deployment. Software-based self-test is a promising complement to existing scan-chain based reliability enhancement techniques in that it can be better integrated into the system operation with little or no interference.

A prototype has been implemented to validate the proposed self-test program generation methodology. Preliminary fault coverage results are encouraging. Further evaluation on RISC-V processors is ongoing. At the same time, we are investigating test program compaction techniques to reduce the memory footprint and optimizing the template generation flow.

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Activity

NTU GICE Hosted IEEE GLOBECOM 2020, the Flagship Conference of IEEE Communications Society

Prof. Kwang-Cheng Chen introducing keynote speakers.

After 18 years, IEEE Global Communications Conference (GLOBECOM) was hosted again in Taipei in December 2020 by NTU GICE. At the time of the pandemic of COVID-19 when most conferences turned virtual, IEEE GLOBECOM 2020 became the first hybrid flagship conference of IEEE Communications Society (ComSoc) thanks to Taiwan's great defense against COVID-19. IEEE GLOBECOM 2020 attracted more than 2000 people from over 60 countries attending the virtual part of the conference on December 7 to 11, 2020, and more than 500 people attending the in-person part which took place at the Taipei International Convention Center (TICC) on December 8 to 10. Themed "Communications for Human and Machine Intelligence" and taking place right at the launch of 5G networks and services, IEEE GLOBECOM 2020 featured not only a high-quality technical program but also 5G, IoT and AI technology exhibition by 18 leading telecom companies such as Chunghwa Telecom, Mediatek, Foxconn, Qualcomm, Ericsson, Cisco, etc. To promote these technologies to the general public, the on-site technology exhibition of IEEE GLOBECOM 2020 was opened to the general public free of charge on December 9 afternoon and December 10, and attracted over 400 people.

NTU GICE is proud to be the driving force behind IEEE GLOBECOM 2020, with Prof. Kwang-Cheng Chen (past GICE Director) leading the executive team, Prof. Hsuan-Jung Su (current GICE Director) leading the technical program committee, Prof. Hung-Yu Wei and Prof. Che Lin coordinating the industry forum and exhibits. IEEE GLOBECOM 2020 received over 2800 paper submissions from more than 70 countries, and accepted 1104 among its technical symposia and workshops. In addition to the technical paper presentations, it had 6 keynote speeches delivered by Dr. Rick Tsai, CEO of Mediatek, Prof. Murial Medard, MIT, Prof. Jay Lee who is also a Vice Chairman of Foxconn, Prof. David Tse, Stanford University, Mr. William Xu, Director of Board & President of the Institute of Strategy Research, Huawei, Dr. Chau-Young Lin, President, Chunghwa Telecomm Laboratories, 9 executive talks delivered by CEOs and CTOs of several telecom companies around the world, 24 tutorials on emerging topics, 19 workshops (including a special workshop on communications and networking technologies for responding to COVID-19), 30 industry forums, panel discussions, presentations, and 73 technology exhibition booths. The success of IEEE GLOBECOM 2020 showcased the strength of Taiwan's academia and industry on 5G, IoT, AI, e-health, etc., and provides a reference model for future hybrid conferences of IEEE.

Director Hsuan-Jung Su presenting an appreciation trophy to Executive Forum speaker, Dr. Chee Ching, President of FarEasTone.

Invited talk

Topic: Distributed Consensus Learning for PCA and Support Vector Machines
Lecturer: Professor Yuh-Jye Lee

Nowadays, machine learning performs astonishingly in many different fields. The more data we have, our machine learning methods show better results. However, in some cases, the data owners may not want to or not allow to share the data they have. On the other hand, we may encounter extremely large data sets that even cannot be stored in a single machine. In order to deal with these two problems, we propose the distributed consensus framework and apply this framework to principal component analysis, PCA and linear and nonlinear Support Vector Machines. This framework is known as Federated Learning. Imagine that we have many local working units and a central master, and each working unit owns its data. The framework allows each local working unit to work on its own data and submits the machine learning model to the central master. The central master will fuse the models collected from the local working units and then broadcast to the local working units. After certain iterations, we will have a model like the one generated by pooling all data together. Thus, the framework includes the following two merits. First, it keeps the privacy of data, for the local working units never share their data are to the central master or other local working units. Besides, when we confront a large dataset, which is hard to store in a single server, this framework may utilize many computational servers to work together to train the machine learning model using the entire dataset.

Dr. Yuh-Jye Lee received the PhD degree in Computer Science from the University of Wisconsin-Madison in 2001. Now, he is a research fellow at the Research Center for Information Technology Innovation, Academia Sinica and serves as the CEO of Taiwan Information Security Center. He also is a professor of the Department of Applied Mathematics at National Chiao-Tung University. His research is primarily rooted in optimization theory and spans a range of areas including network and information security, machine learning, data mining, big data, numerical optimization and operations research. During the last decade, Dr. Lee has developed many learning algorithms in supervised learning, semi-supervised learning and unsupervised learning as well as linear/nonlinear dimension reduction. His recent major research is applying machine learning to information security problems such as network intrusion detection, anomaly detection, malicious URLs detection and legitimate user identification. He also works on online learning algorithms for dealing with large scale datasets, time series data and behavior based anomaly detection for the needs of big data and IoT security problems. Recently, he turns his research attention on federated learning, adversarial machine learning and disinformation prevention.

Corner of student news

Welcome to join IEEE NTU Student Branch!

Article by Xu, Rei-Fu

The Institute of Electrical and Electronics Engineers, popularly known as IEEE, is an international association for electronic engineering, electrical engineering, and associated disciplines. It was first established in 1963, which has already become the largest professional technical organization in the world, with 420,000 members from 175 countries, including academia and industries.

The Student Branch of the Institute of Electrical and Electronics Engineers at the National Taiwan University (IEEE NTUSB) is officially registered under the IEEE Taipei Section. In 2020, IEEE NTUSB resumed operation by a group of graduate students from diverse backgrounds of colleges of EECS. We hope to facilitate social interaction and academic exchange among various domains, providing opportunities to meet and learn from fellow IEEE Student and Graduate Student Members and engage with professional IEEE members locally.

As long as you're interested in EECS-related professional knowledge, we sincerely welcome any NTU graduate or undergraduate student to join us. You can choose to join us as volunteers, regular members, or branch officers. For regular members, you need to complete official registration on the IEEE website. We will provide exclusive opportunities such as company visits or special guest speeches for regular members only. If you have more ideas about student branch organization, you can also join as branch officers and participate in program committee, publicity committee, or even run for the election of branch chair in the future!

Although due to the severe situation of COVID-19 recently, we will still hold virtual seminars and interesting interviews on different social media platforms like YouTube and Podcast. Please refer to the following information:

- Fill out the registration form: https://ppt.cc/fGppLx
- Follow us on Facebook Fan page: https://www.facebook.com/ieeentu.taipei
- Contact us: ieeentustudentbranch@gmail.com

Our first NTUSB Officers meeting after resuming operation

IEEE NTUSB Member Recruit Orientation

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